AMENDMENTS TO THE CLAIMS

1-27 (Canceled)

28. (Currently amended) An array of semiconductor packages, comprising:

a substrate having upper and lower surfaces, one of said upper and lower surfaces including a first plurality of grooves dividing said substrate into a plurality of segments;

a plurality of semiconductor dies provided at the other of said upper and lower surfaces of said substrate, each semiconductor die being substantially aligned with a segment; and

an encapsulant over said plurality of semiconductor dies, said encapsulant having a second plurality of grooves substantially aligned with said first plurality of grooves.

29. (Cancelled)

30. (Cancelled)

31. (Cancelled)

32. (Cancelled)

33. (Cancelled)

34. (Previously presented) The array of semiconductor packages of claim 28, wherein each of said plurality of semiconductor dies is electrically connected to a respective segment of said substrate.

35. (Withdrawn) A method of forming an array of semiconductor packages, said method comprising:

dividing a substrate into a plurality of segments by forming a first plurality of grooves on said substrate;

forming an array of semiconductor dies over said plurality of segments, each

semiconductor die formed to be substantially aligned with a segment; and

forming an encapsulant having a second plurality of grooves over said array of semiconductor dies.

36. (Withdrawn) The method according to claim 35, wherein said step of forming an encapsulant having a second plurality of grooves is performed such that said second plurality of grooves are substantially aligned with said first plurality of grooves.

37. (Withdrawn) The method according to claim 35, wherein said step of forming an encapsulant having a second plurality of grooves comprises:

providing an upper member over said array of semiconductor dies, said upper member surrounding, and forming a cavity around, each semiconductor die;

providing a resin in said cavity; and

removing said upper member.

38. (Withdrawn) The method according to claim 35, wherein said first plurality of grooves is formed on an upper surface of said substrate.

39. (New) The array of semiconductor packages of claim 28, wherein at least one of said first plurality of grooves has a depth of about 1 millimeter to about 3 millimeters.